**Сводный отчет использования ресурсов микросхемы Spartan3E при моделировании нейросети Элмана**

**Дискретная модель сети Элмана (4 входа, 8 нейронов, 9 бит/коэффициент)**

Design Statistics

# IOs : 443

Cell Usage :

# BELS : 2485

# GND : 1

# LUT2 : 34

# LUT2\_L : 8

# LUT3 : 413

# LUT4 : 588

# MULT\_AND : 64

# MUXCY : 640

# MUXF5 : 16

# VCC : 1

# XORCY : 720

# FlipFlops/Latches : 14

# FD : 2

# FDE : 9

# FDRS : 1

# FDS : 2

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 442

# IBUF : 437

# OBUF : 5

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Device utilization summary:

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Selected Device : 3s500eft256-5

Number of Slices: 582

Number of Slice Flip Flops: 14

Number of 4 input LUTs: 1043

Number of IOs: 443

Number of bonded IOBs: 443

Number of GCLKs: 1

Minimum period: 22.442ns (Maximum Frequency: 44.560MHz)

Minimum input arrival time before clock: 22.462ns

Maximum output required time after clock: 37.648ns

Maximum combinational path delay: 37.668ns

**Непрерывная модель сети Джордана (4 входа, 8 нейронов, 32 бит/коэффициент)**

Design Statistics

# IOs : 1547

Cell Usage :

# BELS : 9233

# GND : 1

# INV : 6

# LUT2 : 38

# LUT3 : 1754

# LUT4 : 2080

# MULT\_AND : 248

# MUXCY : 2542

# MUXF5 : 3

# VCC : 1

# XORCY : 2560

# FlipFlops/Latches : 13

# FD : 2

# FDE : 8

# FDRS : 1

# FDS : 2

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 1546

# IBUF : 1541

# OBUF : 5

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Device utilization summary:

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Selected Device : 3s500eft256-5

Number of Slices: 2031

Number of Slice Flip Flops: 13

Number of 4 input LUTs: 3878

Number of IOs: 1547

Number of bonded IOBs: 1547

Number of GCLKs: 1

Minimum period: 26.612ns (Maximum Frequency: 37.578MHz)

Minimum input arrival time before clock: 26.450ns

Maximum output required time after clock: 41.349ns

Maximum combinational path delay: 41.188ns